

Why that 47 uF capacitor drops to 37 uF, 30 uF, or lower

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Abstract

There are a couple of reasons why the capacitance value marked on the device you have, may not read anywhere near that value in the circuit application in which it is intended. The two major contributors to this are the capacitance roll-off with increased frequency exhibited by electrolytic capacitors, and voltage sensitivity (both ac and dc voltages) of capacitance associated with ferroelectric dielectric ceramic capacitors. Capacitance roll-off is a frequency related phenomenon that is dependent upon ESR and capacitance and results in a frequency limit for these larger capacitance devices. Cap roll-off is being addressed by decreasing design ESR. The voltage coefficient of capacitance for the ferroelectric ceramic capacitors is a phenomenon that is becoming ever more critical as dielectric thickness is reduced in order to increase capacitance in smaller size, lower voltage devices. This effect is also noticeable in the larger cases and with more traditional voltage values of ferroelectric ceramic product offerings. Additional changes in capacitance for ferroelectric ceramic capacitors are attributable to capacitance change with changing temperature as well as with the decay of capacitance with time.

This topic has been discussed in previous papers. This paper is a culmination of many of those papers in order to provide a summary for the reader.

Capacitance versus Temperature

This dependence is probably the most widely understood aspect of capacitance deviation from nominal values. Some capacitor types are notorious for their severe dependence of capacitance on temperature. In the realm of multilayer ceramic capacitors (MLCC), dielectric types of Y5V and Z5U allow deviations in capacitance from the room temperature value of -82% and -56%, respectively over their specified temperature ranges (from -30°C to 85°C, and from -10°C to 85°C respectively).¹ The three character code of the MLCC, defines the temperature range (first two characters) and the allowable change in capacitance over that temperature range (defined by the third character). Class 2 capacitors are allowed to change no more than +/-15% over the designated range, while Class 3 dielectrics change more than +/-15% over the designated temperature range. Both of these types of ceramic dielectric materials are ferroelectric, non-linear dielectrics having dielectric constant (K) values that are sensitive to temperature and other environmental factors, while Class 1 capacitors are made with linear or paraelectric dielectric materials and are generally temperature stable or temperature compensating in a predictable and specified manner. The most popular designation for ceramic Class 1 capacitors is the COG designation which changes very little (<+/- 30 ppm/°C) over the designated temperature range (-55°C to +125°C). A summary of the dielectric specifications for Class 1 and Class 2 dielectrics is given in Table 1 and in Table 2.

Table 1. Specifications for Class 1 dielectrics.

| Significant Figure of Temperature Coefficient | | Multiplier of Temperature Coefficient | | Tolerance of Temperature Coefficient | |
|---|--------|---------------------------------------|--------|--------------------------------------|--------|
| PPM/°C | Symbol | Multiplier | Symbol | PPM/°C | Symbol |
| 0.0 | C | -1 | 0 | ±30 | G |
| 0.3 | B | -10 | 1 | ±60 | H |
| 0.9 | A | -100 | 2 | ±120 | J |
| 1.0 | M | -1,000 | 3 | ±250 | K |
| 1.5 | P | -10,000 | 4 | ±500 | L |
| 2.2 | R | +1 | 5 | ±1,000 | M |
| 3.3 | S | +10 | 6 | ±2,500 | N |
| 4.7 | T | +100 | 7 | | |
| 7.5 | U | +1,000 | 8 | | |

Table 2. Specifications for Class 2 and Class 3 dielectrics.

| First Letter | Lower Temp Use Rating (C) | Middle Digit | Upper Temp Use Rating (C) | Last Letter | Maximum Cap Shift from 25°C Value (%) |
|--------------|---------------------------|--------------|---------------------------|-------------|---------------------------------------|
| X | -55 | 2 | +45 | A | +/- 1 |
| Y | -30 | 4 | +65 | B | +/- 1.5 |
| Z | +10 | 5 | +85 | C | +/- 2.2 |
| | | 6 | +105 | D | +/- 3.3 |
| | | 7 | +125 | E | +/- 4.7 |
| | | 8 | +150 | F | +/- 7.5 |
| | | 9 | +200 | P | +/- 10.0 |
| | | | | R | +/- 15.0 |
| | | | | S | +/- 22.0 |
| | | | | T | +22/-33 |
| | | | | U | +22/-56 |
| | | | | V | +22/-82 |

Class 2

Class 3

The relative temperature response of each Class of ceramic capacitors is shown in Figure 1. The severity of temperature change generally parallels the severity of capacitance change with applied dc bias as discussed later in this paper. Both of these factors are largely dependent upon the room temperature K of a given material. In general, the K of Class 3 dielectrics (~6,000 to ~25,000) is considerably higher than the K of Class 2 dielectrics (~1,000 to ~6,000), which is considerably higher than the K of most Class 1 dielectrics (~3 to ~1,000).

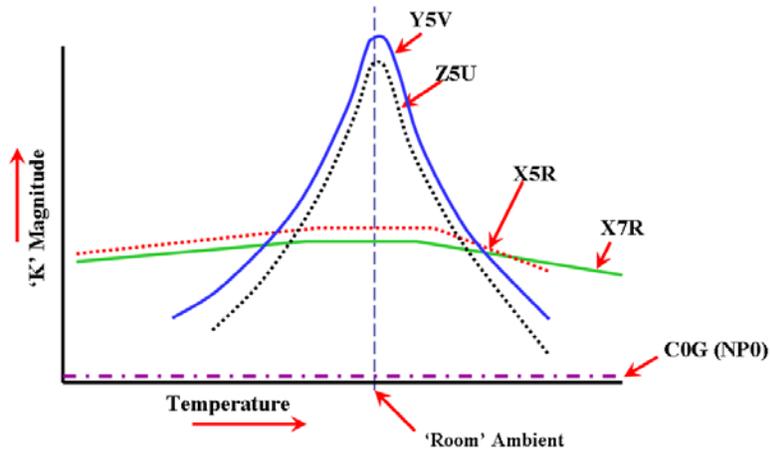


Figure 1. Temperature coefficients of ceramic capacitors.

Thus, there is a trade-off between K and temperature sensitivity, as well as voltage sensitivity as discussed below. The circuit designer must choose dielectrics according to his or her application because of this. An application requiring bulk capacitance with a high capacitance per unit volume, such as microprocessor decoupling in a cell phone or other hand held device, is generally suited to a Class 2 or Class 3 dielectric, while an application requiring excellent temperature stability or predictable temperature compensation, such as filtering or timing, requires a Class 1 dielectric. Use of Class 1 dielectrics comes at the expense of volumetric efficiency however, due to the relatively low K values of Class 1 dielectrics. Table 3 illustrates the maximum capacitance available within several case sizes of MLCC vs. dielectric Class for comparison.

Table 3. Maximum capacitance comparison between dielectric classes.²

| Volumetric Efficiency Comparison by Dielectric (25 V rated) | | | | |
|--|-------------------------|-------------------|--------------------------------------|----------------|
| Case Size | Capacitance (pF) | | % Capacitance (Class 1 Basis) | |
| | Class 1 | Class 2 | Class 1 | Class 2 |
| 0402 | 1,000 | 47,000 | 100% | 4700% |
| 0603 | 10,000 | 220,000 | 100% | 2200% |
| 0805 | 33,000 | 1,000,000 | 100% | 3030% |
| 1206 | 100,000 | 4,700,000 | 100% | 4700% |
| 1210 | 220,000 | 10,000,000 | 100% | 4545% |

Frequency Dependent Capacitance

The electrolytic capacitors (aluminum, wet and solid and tantalum, wet and solid, as well as niobium, solid) all suffer from a loss of capacitance with increasing frequency. This loss is attributable to the resistance-capacitance (RC) ladder that exists within its structure. With a wet aluminum electrolytic capacitor, the first cathode contact to the dielectric is created via the electrolyte solution. This solution, chosen to be highly ionic and conductive as possible, still has a significant amount of resistance associated with it, and is classified as a semiconductor rather than a conductor material.

The high gains of the aluminum sheet are a result of acid etching which creates deep, narrow tunnels in the aluminum foil surface. This effect creates a much larger surface area, and therefore the capacitance is increased by this process. The gain rating of the foil is a ratio of the new, etched surface area of the foil to the old surface area (prior to etching). Gains as high as 300 are typical for low-voltage, etched foils. The surface of the foil, including the tunnel surface created during the etching process, is then oxidized or anodized to create an insulating dielectric film made of alumina (Al₂O₃). The anode contact to the dielectric is the aluminum foil that was etched to form the structure described. The other side of the alumina is the cathode contact. The cathode is achieved using a wet electrolyte. The deep sections or tunnels of the foil are penetrated by the electrolyte. This leads to a long and narrow path for charging current which increases the effective charging/discharging resistance. The conductivity of the electrolyte also plays a major part in determining this resistance. A physical representation of the RC-Ladder described above is illustrated in Figure 2. The deeper the electrolyte has to penetrate into the tunnel to make contact with an incremental capacitance, the higher the resistance.

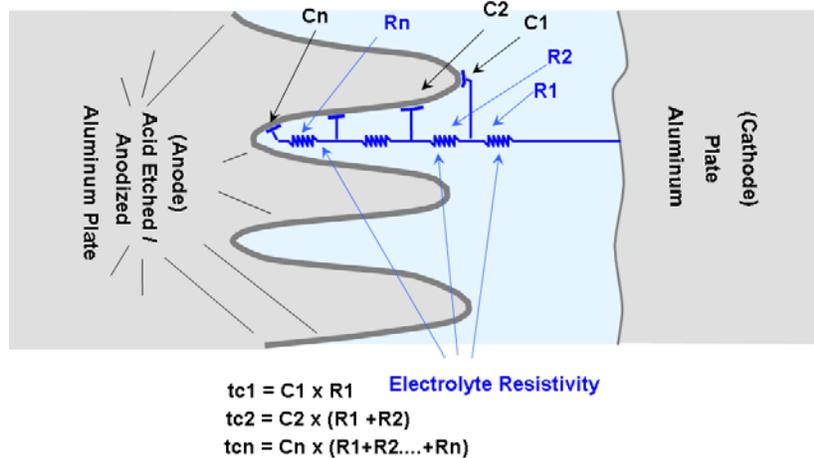


Figure 2. RC-Ladder in wet aluminum electrolytic capacitor.

Electrically this creates a typical RC-Ladder network (Figure 3).³ In lower frequencies, the cumulative incremental capacitances respond to the circuit stimulus efficiently and the capacitance is the value expected from the design. However, as frequency increases, the lumped resistance (i.e., $R_1 + R_2 + R_3 + \dots + R_n$) to the deepest capacitance element (C_n) within the etched foil structure becomes so high that these deep capacitive units cannot respond within the time period of the frequency of the electrical stimulus as their associated RC time constants (tc_n) approach or exceed the time period of the electrical stimulus. As frequency increases, the period of the stimulus decreases and more and more of the capacitance elements stop responding to the stimulus (C_{n-1} , C_{n-2} , C_{n-3} , ...). Because of this, the apparent capacitance drops as frequency is increased. Eventually, only the capacitive elements closest to the terminations nearest the source of the stimulus can respond by charging and capacitance roll off becomes dramatic as the apparent capacitance is relative low compared to the design capacitance.

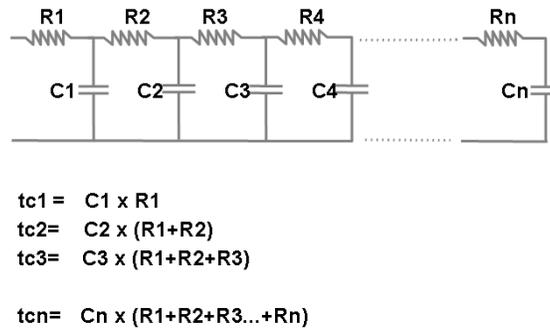


Figure 3. RC-Ladder circuit network.⁴

Typical capacitance versus frequency curves for wet electrolyte aluminum electrolytic and for solid electrolyte tantalum (Ta) electrolytic capacitors are shown in Figure 4. The plot on the left is the measured capacitance for a wet aluminum electrolytic capacitor for several temperatures, and the plot on the right is the measured capacitance for a solid tantalum capacitor at these same temperatures. These measurements show the frequency effect as well as the temperature effect of capacitance upon these two types of electrolytic capacitors.

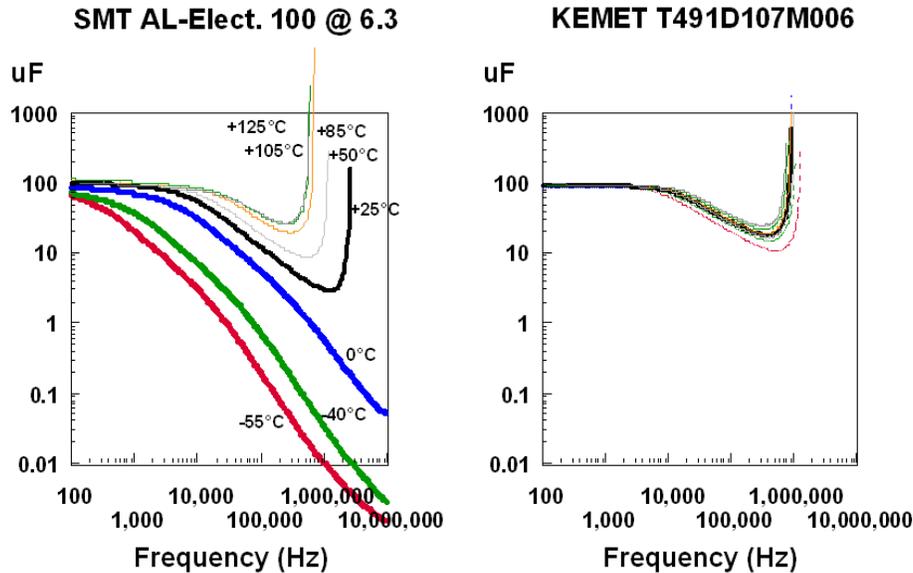


Figure 4. Capacitance versus frequency for wet aluminum electrolytic and solid tantalum capacitors.

Capacitance loss in the aluminum capacitor begins just above 10 kHz at 105°C and 125°C. As temperature is lowered, the loss of capacitance begins at lower frequencies. Additionally, figure indicates that the change in capacitance with temperature for the aluminum electrolytic capacitor and for the tantalum capacitors at low frequencies is nearly linear with temperature. Capacitance increases approximately 10% near 125°C, and decreases approximately 10% at -55°C (Figure 5).

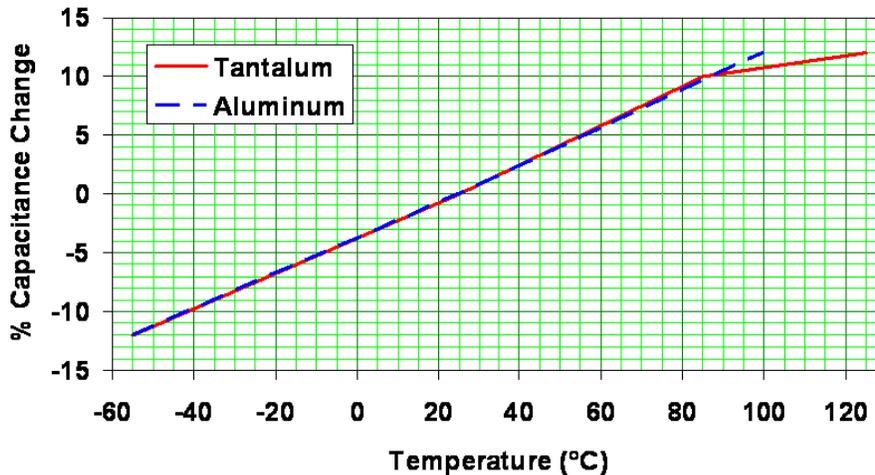


Figure 5. Capacitance versus temperature for wet aluminum and solid tantalum capacitors at 120 Hz.

Looking at the capacitance versus frequency response for the tantalum on the right of Figure 4, and in the lower frequencies, the $\pm 12\%$ changes from Figure 5 are lost in the resolution of the scale. The enormous changes for the aluminum at 100 kHz (Figure 4) compared to the results in Figure 5, tells us that more is changing than just the capacitance in this response.

In the Ta device, the RC-Ladder is illustrated in Figure 6. The first element in the RC-Ladders is created by the cathode material (MnO_2) which penetrates the porous pellet anode structure. As the MnO_2 penetrates the pores to make contact with the distributed capacitive elements (elements of the dielectric Ta_2O_5 anodized film in this case), the resistance increases as the charge/discharge path traverses into the center of the pellet. For the deep capacitor elements the resistance is much higher than the resistance to the outer capacitor elements nearer the outside surface of the pellet, as illustrated in

Figure 6. The resistance of the MnO₂ is high compared to the resistance the tantalum anode material. Because of this, the electrical network illustrated in Figure 3 applies well here also.

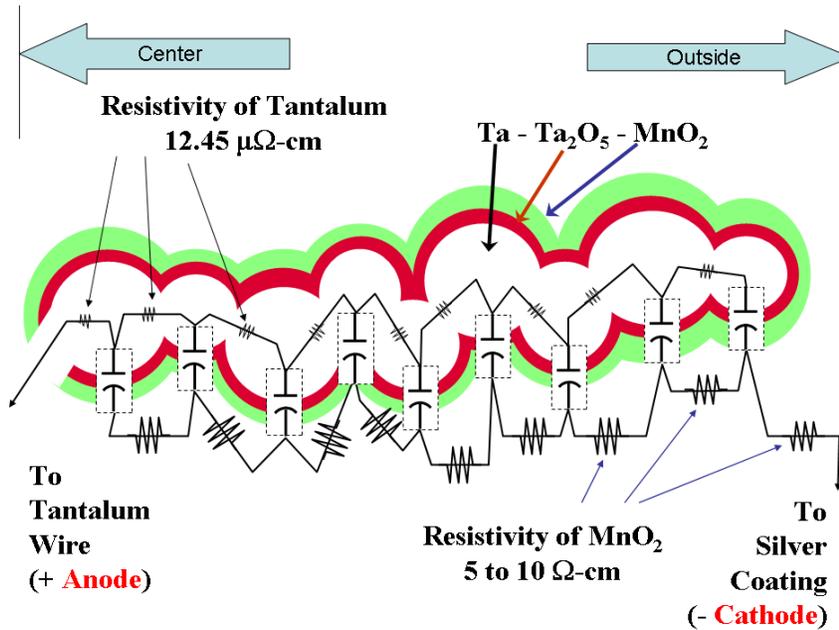


Figure 6. RC-Ladder physical structure in tantalum capacitor.

With these devices it is possible to mathematically strip the ESR readings out of the impedance measurements as shown in Figure 7. The figure indicates that ESR changes dramatically with decreasing temperature in a wet aluminum electrolytic capacitor, and relatively little for a solid electrolytic tantalum capacitor.

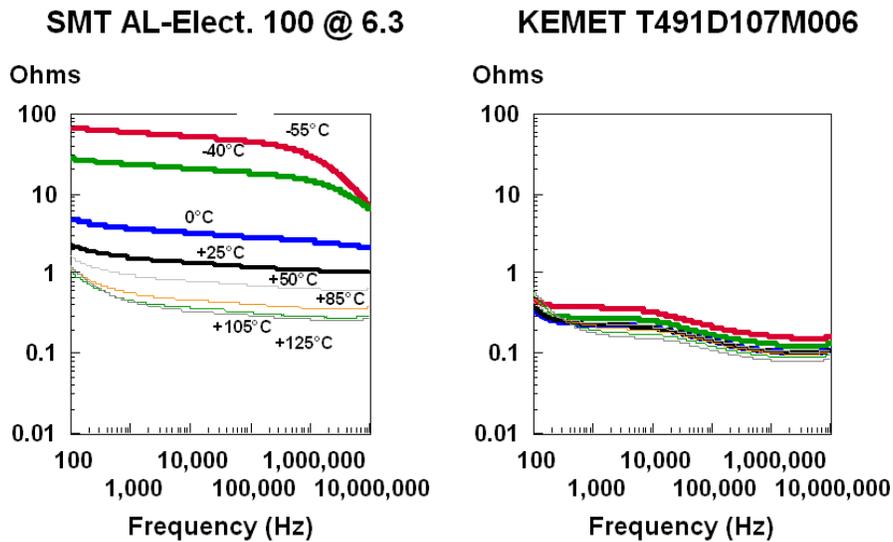


Figure 7. ESR versus frequency and temperature for wet aluminum and solid tantalum capacitors.

A major contributing factor to the increase in the ESR of the aluminum electrolytic capacitor is that the resistivity of the electrolyte changes by a factor close to 100 in going from 25°C to -55°C. Thus, the drastic changes in capacitance observed in the wet electrolytic aluminum capacitor is largely due to the change in the resistance of the electrolyte with changing temperature and not so much to the change in capacitance of the dielectric with changing temperature. It is evident from Figure 4, that the RC-Ladder stops having an effect on the solid electrolyte tantalum capacitor from just below

10 kHz to 100 Hz (the limit of the measurements). In contrast, the effects on capacitance of the RC-Ladder for the wet aluminum electrolytic capacitor appear to continue to frequencies below 100 Hz (Figure 4).

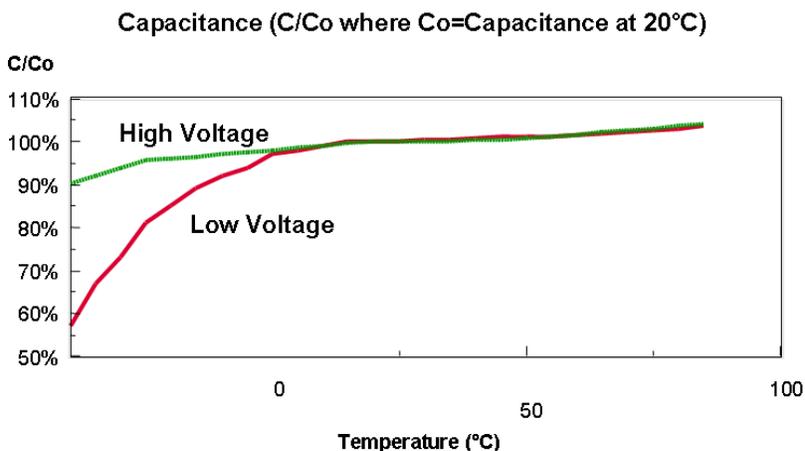


Figure 8. Capacitance change for wet aluminum electrolytic versus temperature.

In Figure 8, a plot of capacitance versus frequency is shown for high voltage and low voltage aluminum wet electrolytic capacitors. The difference noted between high and low voltage is not due to the dielectric responding differently, but to the fact that the RC-Ladder dominates the ESR in the high surface, porous formed film used in the low voltage capacitor. The diameter of the etched pore tunnels for the low voltage film is much tighter, resulting in higher ESR for the low voltage capacitor. It is misleading to attribute this effect to the alumina dielectric.

ESR as a Factor for Capacitance Roll-off

This loss of capacitance in electrolytic capacitors can be offset with reductions in ESR. Consider process and material changes that have resulted in reductions in ESR of tantalum capacitors (Figure 9). With the initial tantalum capacitor (T491), lower ESRs were first achieved via material and process changes (T495), then by physical changes (T510), and finally by material changes (T530). The achievement of lower ESRs resulted in shifting the capacitance roll-offs to higher frequencies in each case.

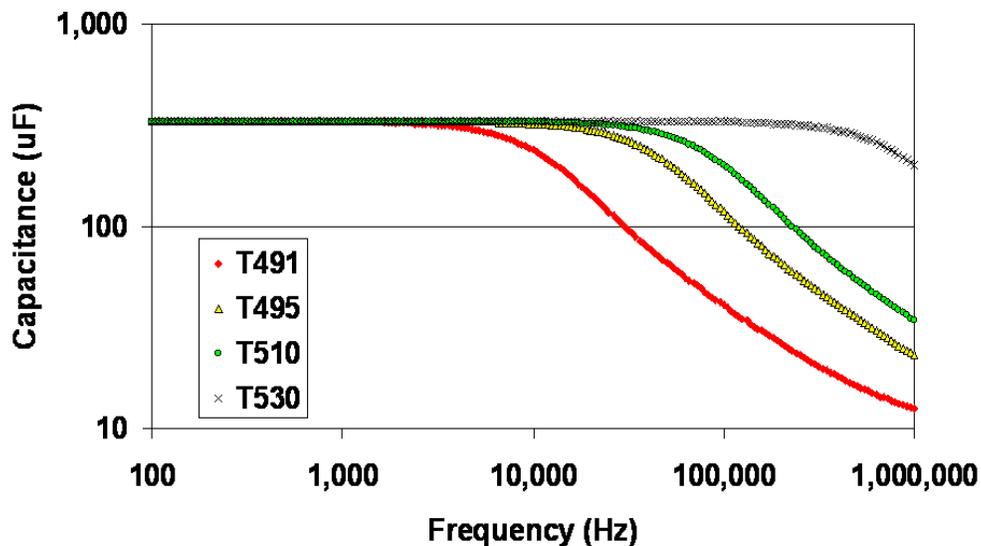


Figure 9. Changing capacitance roll-off by changing ESR.

Using the T491 device as the starting point, the low ESR evolution began by offering the T495 which utilizes the same materials set, but the tantalum powders were larger creating larger pores, and the impregnation of the anode with the cathode material (MnO_2) is modified to create a denser, thicker deposition of this material into the pellet structure. As a result the ESR is lower and the capacitance roll-off is moved to higher frequency.

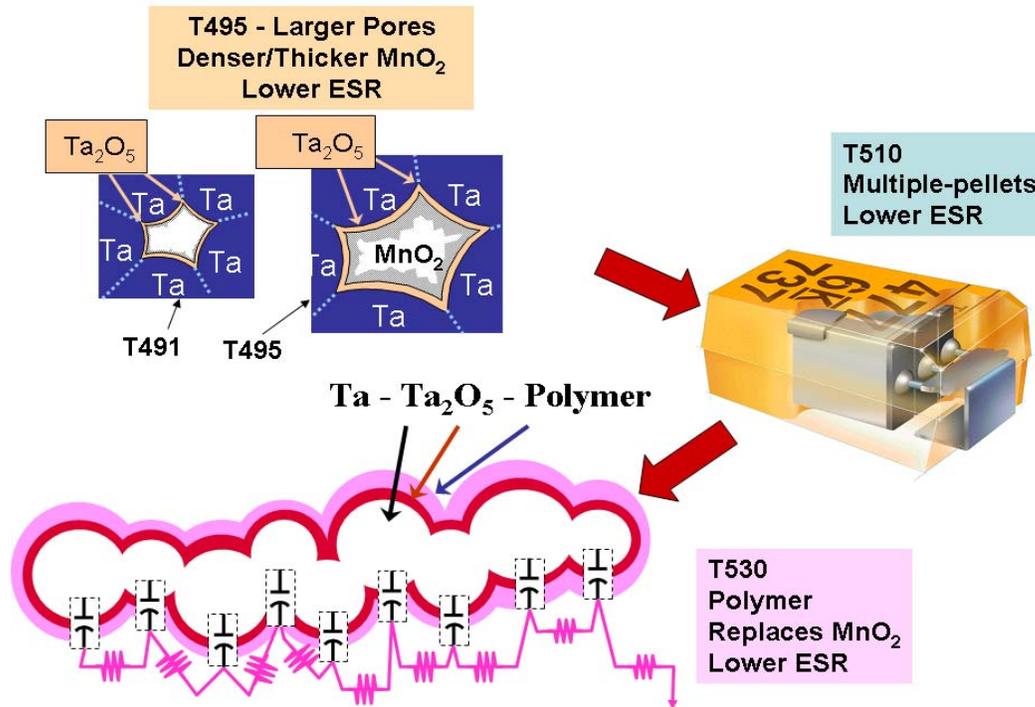


Figure 10. Progression to lower ESR from T495 to T510, to T530.⁴

In the T510, multiple anode pellets then replaced a the single anode pellet in the T495 devices. The penetration depth of the cathode to the center of the pellet has been reduced as well. The multiple anode pellets in parallel reduce the electrical resistance of the charge/discharge current path according to the rule of resistors in parallel. This, combined with the reduced distance to the center of the anode results in further reduction in ESR, moving the capacitance roll-off to an even higher frequency than either the T491 or the T495 device as illustrated in Figure 9. In the T530 device, the cathode material is changed from MnO_2 to a conductive polymer having significantly lower resistivity than MnO_2 . This material impregnated into the parallel anode pellet structure of the T510 results in further reduction of ESR and, again capacitance roll-off is moved to higher frequency.

Capacitance Factored by DC Bias Voltage

Unique to Class 2 and 3 ceramic capacitors is a potentially large change in capacitance created by applied voltage across the device.⁵ Both ac and dc voltages affect K of the dielectric or capacitance in the resulting device. We explain the dc effects first. These effects are NOT attributable to linear, Class 1 C0G (or NP0 for the older readers) dielectrics.

There are four methods of field enhancement or polarization that may take place in a capacitor dielectric material: electronic, atomic, dipole, and space charge. High capacitance per unit volume (CV) Class 2 and 3 ferroelectric, non linear dielectrics such as X7R, X5R, X6S, X7S, X7T, Y5V, etc. all are dominated by the dipole or orientation polarization mechanism.

Four Basic Polarization Mechanisms:

- Electronic
- Atomic
- Dipolar or Orientation
- Space Charge

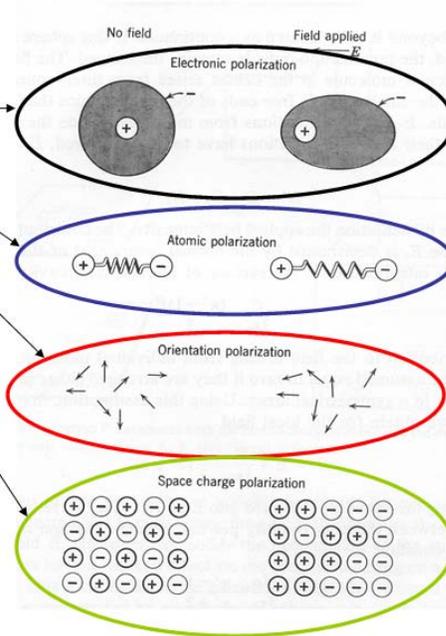
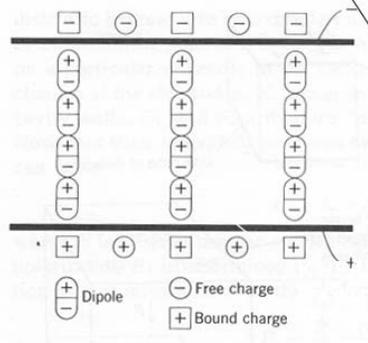


Figure 11. Polarization mechanisms within capacitor dielectrics.⁶

Consider the dipole orientation illustrations shown in Figure 12. At 0 Vdc, the orientation mechanism of the ac voltage has most of the dipoles flipping back and forth with the ac voltage. Applying a dc voltage (X Vdc) locks some of those dipoles in place, preventing the ac voltage from reorienting them. Further increasing the dc bias voltage (5X Vdc) locks up more of the dipoles such that even fewer dipoles within the material reorient with the ac signal, thereby reducing the contribution of the dipoles to the K value, as the dielectric constant is directly related to the number of operant dipoles per unit volume in a material. The more dipoles that align themselves to the applied ac field, the higher the resulting capacitance. Locking up these dipoles lowers the capacitance.

The dc field is experienced by the dipoles is created by two elements: 1. the applied dc voltage, and 2. the thickness of the dielectric. As the dielectric decreases in thickness, the dc field increases at constant applied dc voltage. Applying 3 Vdc to the dielectric within an MLCC that is rated at 4 Vdc will lock up many more dipoles than applying that same voltage to the dielectric within an MLCC that is rated at 10 Vdc since the thickness of the dielectric generally scales with rated voltage of an MLCC device.

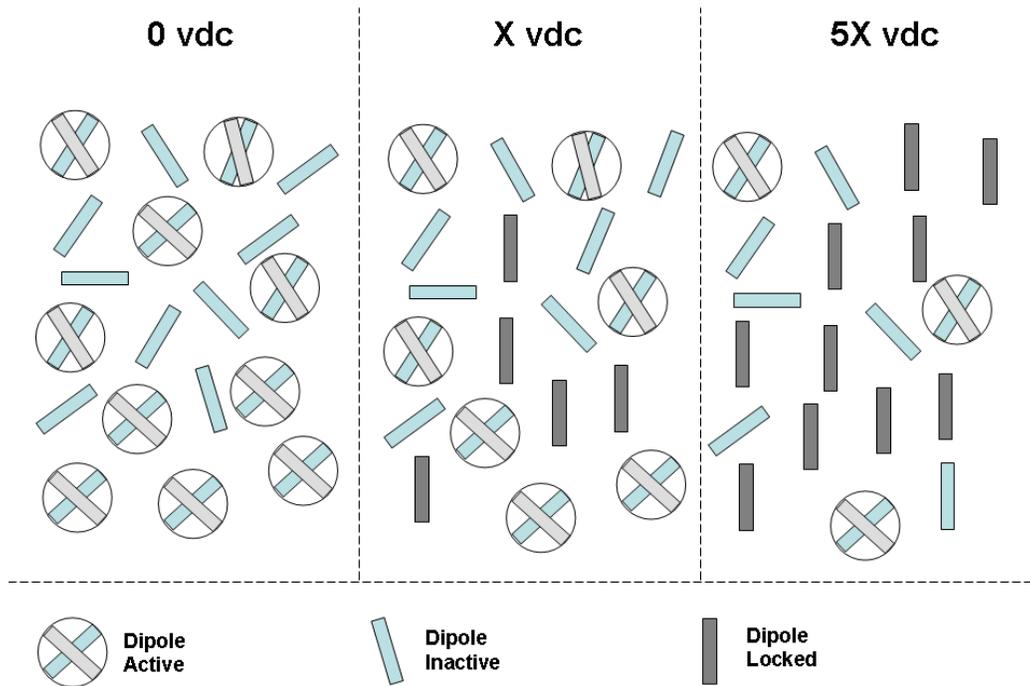


Figure 12. Active dipoles being locked by dc bias.

An example of this effect is given in Figure 13. The figure illustrates the effect of dc voltage on 22 μF MLCCs. Both of these devices are made with X5R rated dielectric, but the voltage ratings and the dielectric thicknesses are different, thus requiring different chip sizes as well. The capacitance loss observed is proportional to the dc field (v/ μm). Since these devices have different dielectric thicknesses, the loss in capacitance is significantly higher for the lower rated voltage, thinner dielectric MLCC at any given voltage.

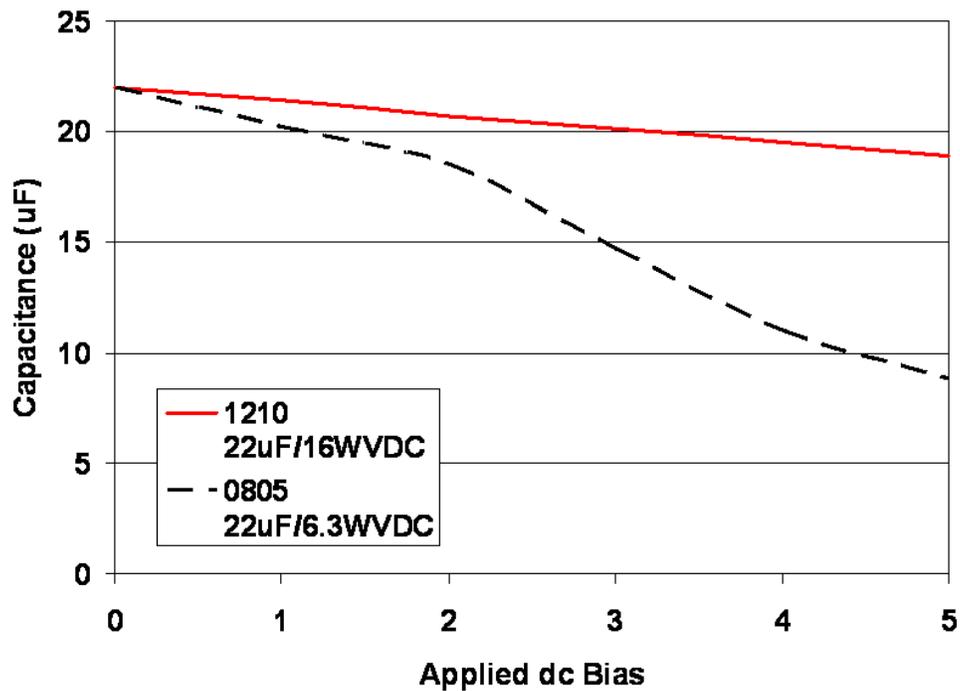


Figure 13. Capacitance versus applied dc voltage – same capacitance, same dielectric.

AC Voltage Effect on Capacitance

With ac voltage, the number of dipoles that align to the field is proportional to the strength of the field. This property is becoming more of a concern as the thickness of the ferroelectric dielectric materials is decreased in order to maximize CV.^{7,8,9,10} As ac voltage is increased, capacitance also increases. However, there is a point with increasing ac voltage that the dipoles begin to be saturated in and further increase in ac voltage does not increase the level of polarization within the dielectric proportionally. This results in a hysteresis behavior the material. The effect of ac field on the level of polarization is non linear. This non-linearity can be quite pronounced and the oriented dipoles may stay locked in their orientation until acted upon by a significant electric field in the direction opposite to their polarization. This hysteresis property may be useful in applications that require a remnant state of polarization, such as in ferroelectric memory. Thus, these ferroelectric, non-linear Class 2 and 3 dielectrics exhibit a hysteresis property, as there is a memory or retention of a portion of the polarization. This memory is measured as a retained charge that may also be known as dielectric absorption or remnant polarization. Some of those dipoles that moved easily under small voltages may now be locked into one orientation state, effectively causing the dipole to appear to be lost. Hysteresis effect typical, of ferroelectric materials, is illustrated in Figure 14.

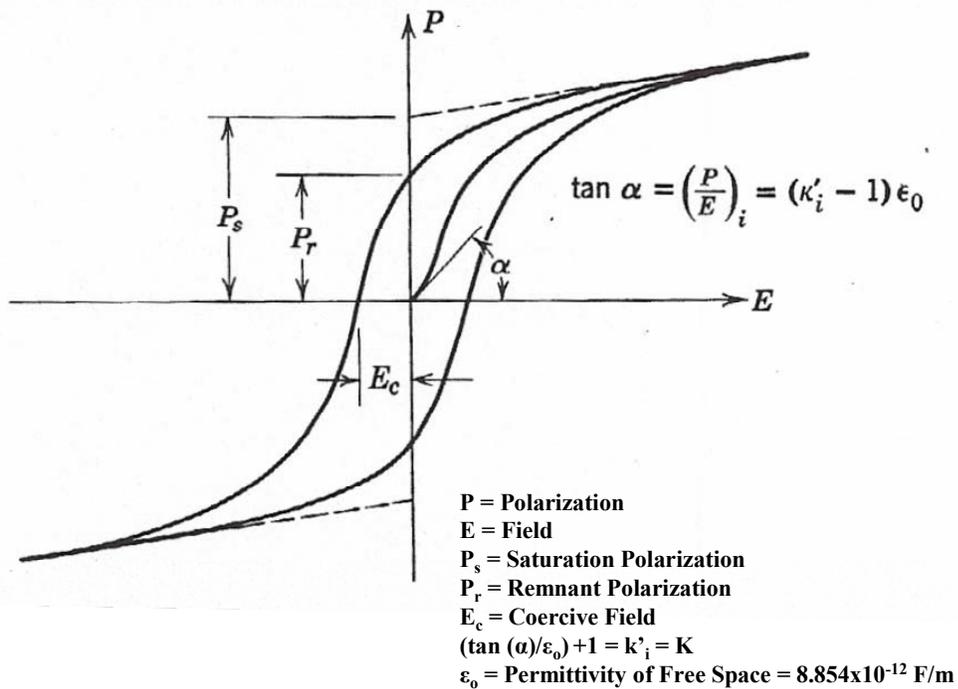


Figure 14. Hysteresis behavior typical of ferroelectric materials (polarization as a function of electric field).¹¹

The illustration of Figure 15, points out these two phases of the response of capacitance with ac voltages. Going from 0.1 Vac to 0.5 Vac, the capacitance increases, but going from 0.5 Vac to 10 Vac, the capacitance is decreasing.

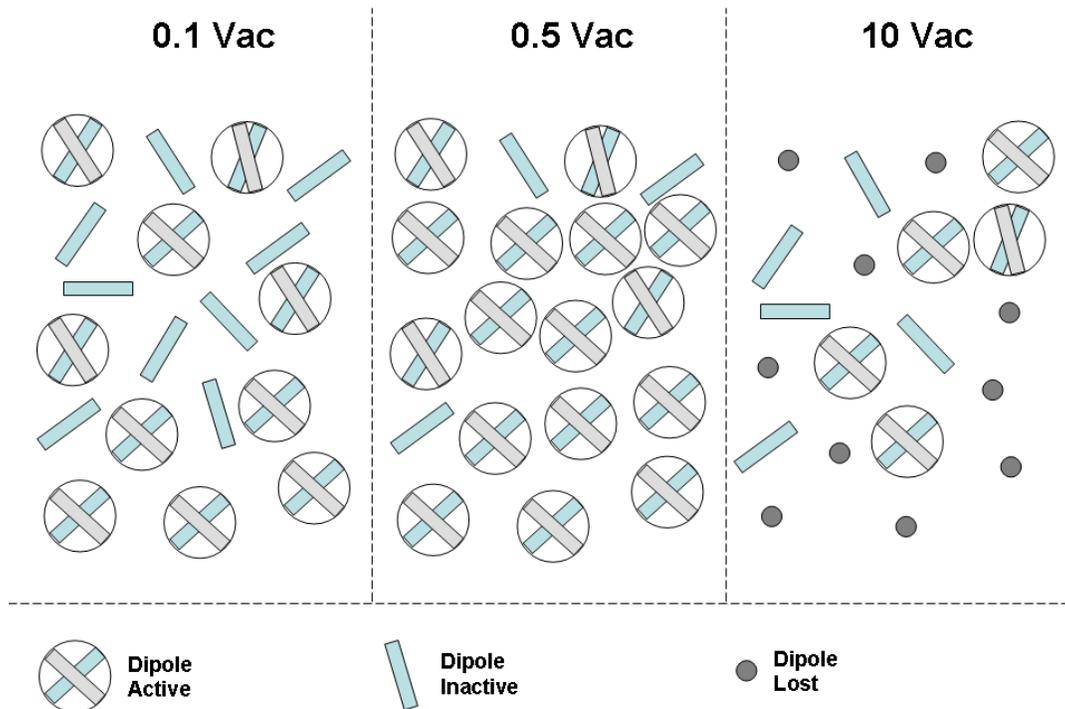


Figure 15. Dipole saturation then loss with increasing ac voltages.

Looking at a plot (Figure 16) of measured capacitance versus changing magnitude of ac voltage details these changes. The variation of ac voltages will be limited in higher frequencies for larger capacitance values as the impedance will be so low in this realm. Although this is true for the high frequency, remember that nominal capacitance and tolerance are measured at lower frequencies, and the voltages used here are higher than those found in typical high frequency applications, and this will cause decay in capacitance.

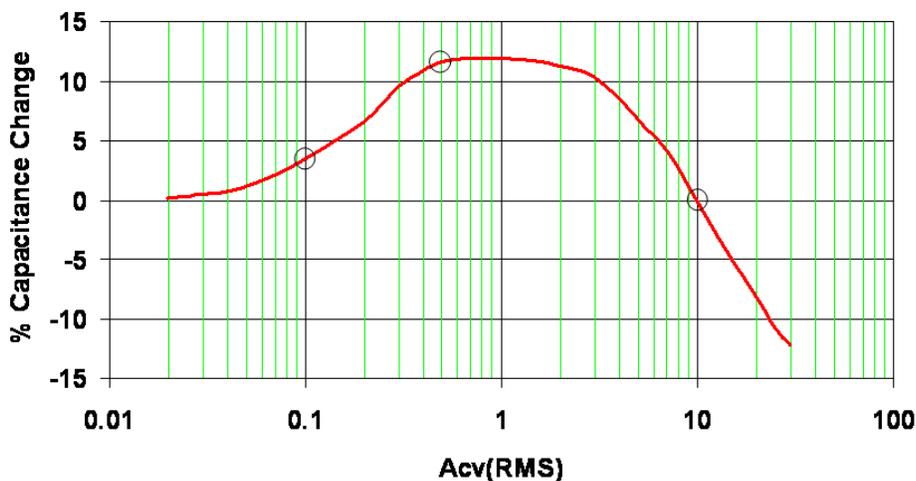


Figure 16. Capacitance versus ac voltage with indications at 0.1, 0.5, and 10 vrms.

Aging – Loss of Capacitance with Time

Another capacitance factor that applies only to MLCCs relates to the loss of capacitance with time. As with voltage coefficients, this characteristic does not apply to the COG (Class 1) dielectric MLCCs. The magnitude of change in

capacitance with time has a slight correlation to the relative magnitude of dielectric constants for the Class 2 and Class 3 dielectric types. This loss of capacitance follows natural decay rules and is usually expressed as a percent per decade. It is related to a transition of the BaTiO₃ crystalline structure. When the heated above the Curie point (>125°C), the structure reverts to a cubic symmetrical structure. Upon cooling, the shape of the unit cell changes to a tetragonal structure and results in a strain in the material. This strain relaxes over time and the dielectric constant decays as well. This decaying capacitance can be reset by heating the device above the Curie point, or above 125°C, for a brief period. The soldering process used to mount MLCC devices to the circuit board creates temperatures above the Curie temperature for a brief time, creating a partial reset of the capacitance.

In Figure 17, the upper and lower tolerances for a ±20% capacitor (i.e., M tolerance) are plotted as well as the change in capacitance of a typical ferroelectric MLCC with time. The aging rate for this device was established to be at 8% per decade-hour, by monitoring capacitance versus time for several batches of this material. The specified tolerance is typically applied to the device at 1,000h of aging post-heat. In order to “guard band” the tolerance, the tolerance limits are typically drawn in at ±19.5% at this time. At times prior to the reference time (1,000 h), the upper capacitance limit actually includes values above +20%, and at times greater than the reference time the lower range of the capacitance distribution may include parts below the -20% limit. If this piece is mounted on a PCB and then subjected to the solder reflow temperatures, the capacitance could “recover” near its fullest state and pieces may appear to be out of tolerance – high. At 1 hour post heat, the ±20% capacitor could show a range of +48.2% and a low limit of -0.2%. Without understanding the mechanism at work, one could easily assume that the pieces were not properly tested and high capacitance units were sent.

What about the other end of the plot? As the times increase beyond 1,000h, how much decay is possible? Looking at 10,000h (just beyond one year or 8,766h), the ±20% capacitor could range from a high tolerance of 9.9% to a low tolerance of -26.0%. Ten years after the 1,000h, may show the tolerance range of this capacitor now from a high of 0.4% to a low of -32.4%. This points out why the Y5V should not be used in systems that are intended for long life (>3 years) applications.

The actual aging rates spelled out in our catalog list the following aging rates:

COG @ 0%, X7R @ 2%, X5R @ 5%, Y5V @ 7%, and Z5U @ 7%

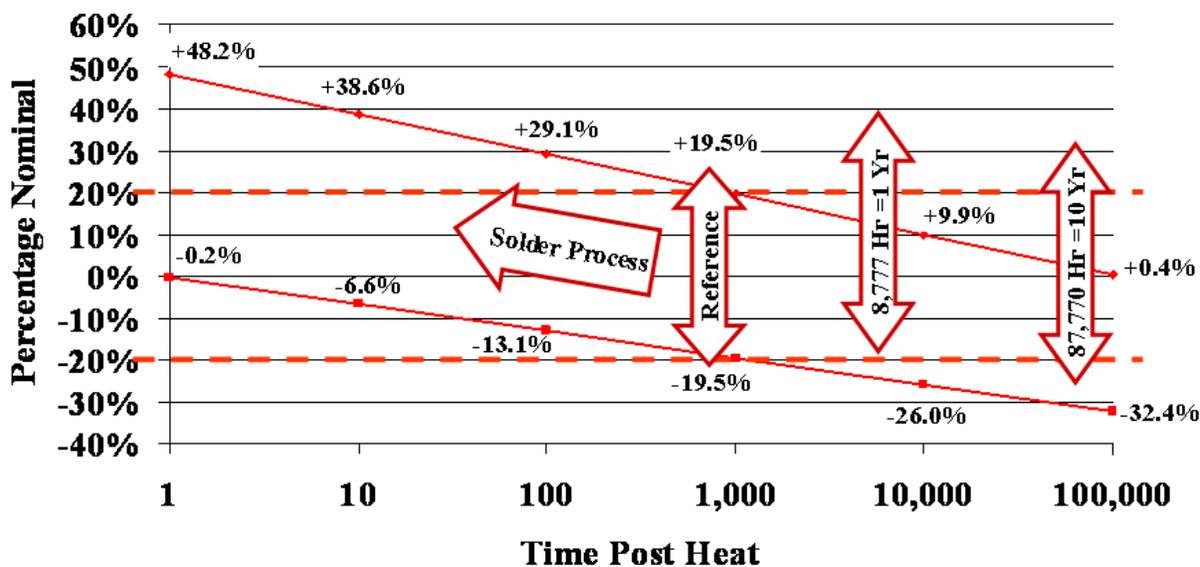


Figure 17. Aging rate (8%/decade-hour) applied to upper and lower tolerances (±20%) for Y5V device.

Summary

Capacitance may be factored by multiple conditions, some environmental and some electrical. The effects of temperature are inherent to the materials used in the dielectrics, with variations of these materials within a specific dielectric type having additional variations possible (e.g., MLCCs with X7R, X5R, Y5V, etc.). For the most part, the details of this temperature dependence are well published and available. The loss of capacitance with frequency in

electrolytics is not as widely known, and will require data made available from the manufacturer. With KEMET, this dependence is detailed in the KEMET_Spice software available on our web site, and may be available from other manufacturers.

The loss of capacitance with time (MLCCs aging) may be found in electrical performance sections of the manufacturers' catalogs. The change of capacitance with ac and dc voltage is probably the least available information. The variation of capacitance with dc voltage is again available in our KEMET_Spice software.

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